a. **Introductory Comments**

Claims 1 – 13 are pending and have been rejected.

Herein, Applicants amend claim 1.

In this Request for Continued Examination, Applicants request reconsideration.

d. Amendments to Claims

1. (currently amended) An apparatus, comprising:

a crystalline substrate having a top surface;

a crystalline semiconductor layer comprising group III-nitride and being located on the top surface, the crystalline semiconductor layer having first and second surfaces, ~~a convex region of the first surface being in contact with the top surface,~~ a plurality of lattice defects having first ends on the ~~region~~ first surface, the second surface being separated from the top surface by semiconductor of the crystalline semiconductor layer, the entire portion of the first surface between the defects being next to the top surface; and

a plurality of dielectric regions located on the second surface, each defect threading the crystalline semiconductor layer and having a second end covered by a different one of the dielectric regions, each dielectric region being distant from the other dielectric regions.

2. (original) The apparatus of claim 1, wherein the crystalline substrate is lattice-mismatched to the crystalline semiconductor layer.

3. (original) The apparatus of claim 1, wherein each dielectric region is a cap covering a single threading defect.

4. (original) The apparatus of claim 3, wherein the caps comprise an oxide of gallium.

5. (original) The apparatus of claim 1, wherein the dielectric regions comprise metal oxide.

6. (original) The apparatus of claim 1, wherein the group III-nitride comprises Ga, Al, or In.

7. (original) The apparatus of claim 2, wherein the lattice-mismatched substrate comprises sapphire.

8. (original) The apparatus of claim 1, wherein a concentration of metal atoms in the lattice defects is higher than in surrounding semiconductor matrix of the crystalline semiconductor layer.

9. (previously presented) The apparatus of claim 1, further comprising a conductor in contact with the second surface and configured to transmit a current to the layer.

10. (original) The apparatus of claim 1, wherein the lattice defects are electrically passivated.

11. (original) The apparatus of claim 2, wherein the top surface is planar.

12. (original) The apparatus of claim 10, wherein the substrate is c-plane sapphire.

13. (original) The apparatus of claim 11, wherein the second surface of the crystalline semiconductor layer is smooth.